

CLAIMS:

We claim:

- 1 1. An apparatus comprising:  
2 an amplifier to generate an output to a load; and  
3 a digital-to-analog converter to drive the amplifier during at least one of powering  
4 up and powering down the amplifier, the digital-to-analog converter to control the  
5 amplifier to ramp the voltage at the output at a predetermined rate to reduce rapid voltage  
6 changes from being sent to the load during the at least one of powering up or powering  
7 down of the amplifier.
- 1 2. The apparatus of claim 1 wherein the output of the amplifier to the load is through  
2 a blocking capacitor, the digital-to-analog converter to control the ramp of the voltage at  
3 the output to at least one of charging the blocking capacitor to a steady-state reference  
4 value at the predetermined rate and of discharging the blocking capacitor from the  
5 steady-state reference value at the predetermined rate.
- 1 3. The apparatus of claim 2 wherein the amplifier to generate an audio output to the  
2 load in which the at least one of powering up and powering down at the predetermined  
3 rate reduces audio pop and click at the load.
- 1 4. The apparatus of claim 1 further comprises a control circuit to generate data sent  
2 to the digital-to-analog converter during at least one of powering up and powering down  
3 the amplifier.
- 1 5. The apparatus of claim 4 wherein the data from the control circuit ramps the  
2 voltage at a substantially linear ramp rate.
- 1 6. An apparatus comprising:  
2 an audio amplifier to generate an output to an audio load;  
3 a digital-to-analog converter to drive the audio amplifier during at least one of  
4 powering up and powering down the audio amplifier, the digital-to-analog converter to  
5 control the audio amplifier to ramp the voltage at the output at a predetermined rate to  
6 reduce audio pop and click from being heard at the load during the at least one of  
7 powering up or powering down of the audio amplifier; and  
8 a control circuit to generate data sent to the digital-to-analog converter during at  
9 least one of powering up and powering down the audio amplifier.

1 7. The apparatus of claim 6 further comprises a clamping switch at an output node of  
2 the audio amplifier to clamp the node to a power return potential, wherein the clamping  
3 switch clamps the output node to the return potential at initiation of a powering up  
4 sequence and releases the clamp when the audio amplifier and the digital-to-analog  
5 converter are substantially fully powered.

1 8. The apparatus of claim 7 wherein the data from the control circuit ramps the  
2 voltage at a ramp rate below frequency heard at the load.

1 9. The apparatus of claim 6 further comprises a clamping switch at an output node of  
2 the audio amplifier to clamp the node to a power return potential, wherein the clamping  
3 switch clamps the output node to the return potential at initiation of a powering down  
4 sequence and releases the clamp when the audio amplifier and the digital-to-analog  
5 converter are substantially turned off.

1 10. The apparatus of claim 9 wherein the data from the control circuit ramps the  
2 voltage at a ramp rate below frequency heard at the load.

1 11. A method to power up or power down an audio amplifier comprising:  
2 sending digital data for digital-to-analog conversion during a powering up or  
3 powering down of an audio amplifier, which generates an output to an audio load;  
4 converting the digital data to drive the audio amplifier; and  
5 using the converted digital data to control the ramping of the voltage at the output  
6 to not exceed a predetermined rate to reduce audio pop and click from being heard at the  
7 load during the powering up or powering down of the audio amplifier.

1 12. The method of claim 11 further comprises ramping the voltage at the output to a  
2 steady-state reference value at the predetermined rate during the powering up of the audio  
3 amplifier.

1 13. The method of claim 12 further comprises the clamping of an output node of the  
2 audio amplifier to a power return potential during powering up and releasing the clamp  
3 when the amplifier is substantially fully powered.

1 14. The method of claim 12 wherein using the converted digital data controls the  
2 ramping of the voltage to a ramp rate below frequency heard at the load.

1 15. The method of claim 11 further comprises ramping the voltage at the output from  
2 a steady-state reference value at the predetermined rate during the powering down of the  
3 audio amplifier.

1 16. The method of claim 15 further comprises the clamping of an output node of the  
2 audio amplifier to a power return potential during powering down and releasing the  
3 clamp when the amplifier is substantially turned off.

1 17. The method of claim 15 wherein using the converted digital data controls the  
2 ramping of the voltage to a ramp rate below frequency heard at the load.

1 18. An integrated circuit comprising:  
2 an audio amplifier to generate an analog output to an audio load, when the audio  
3 load is operably coupled to the integrated circuit;  
4 a digital-to-analog converter to drive the audio amplifier during at least one of  
5 powering up and powering down the audio amplifier, the digital-to-analog converter to  
6 control the audio amplifier to ramp the voltage at the output at a predetermined rate to  
7 reduce audio pop and click from being heard at the load during the at least one of  
8 powering up or powering down of the audio amplifier; and  
9 a control circuit to generate data sent to the digital-to-analog converter during at  
10 least one of powering up and powering down the audio amplifier.

1 19. The integrated circuit of claim 18 wherein the control circuit is a digital signal  
2 processor.

1 20. The integrated circuit of claim 18 further comprises a clamping switch at an  
2 output node of the audio amplifier to clamp the node to a power return potential, wherein  
3 the clamping switch clamps the output node to the return potential at initiation of a  
4 powering up sequence and releases the clamp when the audio amplifier and the digital-to-  
5 analog converter are substantially fully powered.

1 21. The integrated circuit of claim 18 further comprises a clamping switch at an  
2 output node of the audio amplifier to clamp the node to a power return potential, wherein  
3 the clamping switch clamps the output node to the return potential at initiation of a  
4 powering down sequence and releases the clamp when the audio amplifier and the  
5 digital-to-analog converter are substantially turned off.